E2 STATUS REPORTING AND CONTROL SYSTEM
MULTIDIRECTIONAL DATA REGENERATOR
DESCRIPTION

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1. INTRODUCTION

1.01 This section describes the J92618S and J92618R multidirectional data regenerator, hereafter referred to as the regenerator, used in the E2 Status Reporting and Control System.

1.02 This section is reissued to update Fig. 1 through Fig. 4 and to add new references in Part 4. Since this reissue covers a general revision, marginal arrows ordinarily used to indicate changes have been omitted.

1.03 The purpose of the regenerator is to recognize the E2 word start sequence, to retime and reshape the received data signals, and to retransmit this data to the other data networks connected to the regenerator. This process of regeneration eliminates amplitude and envelope delay distortion through timing and reshaping, provides a high signal-to-noise ratio, presets the amplitude of the outgoing signals, and provides complete isolation between all connecting networks.

1.04 The regenerator can be incorporated into an E2 system for two main reasons. First, the regenerator allows a large multipoint data network to be segmented into a number of smaller multipoint data networks. This allows the system to become more manageable from an engineering and maintenance viewpoint. Second, the regenerator can be used in a network which otherwise would be nonexpandable due to the number of links in tandem (see Fig. 1).

1.05 The regenerator has been designed with multidirectional capabilities. It can accept data from any one of eight directions and retransmit the reconstructed data to all other directions; however, data is not transmitted back in the direction from which it was received. The regenerator has been designed on a modular basis and can be equipped to handle from two to eight directions.

1.06 The regenerator can be used only with E2 word formats and only at the 600 bit/second data rate.

2. PHYSICAL DESCRIPTION

2.01 Two versions of the regenerator are available, the J92618S stand-alone version and the J92618R which is collocated with the E2 remote bay. The two versions are discussed separately in the following paragraphs.

A. J92618S Stand-Alone Version

2.02 The basic J92618S L1 stand-alone version of the regenerator (Fig. 2) is equipped for bidirectional transmission (two directions). It consists of seven circuit packs (CPs) contained in one 23-inch wide by 6-inch high shelf, plus a 23-inch wide by 2-inch high jack field for terminating and testing facilities. Each circuit pack performs a specific function or functions as shown in Table A.

Note: Two receive/transmit control circuit packs (CP 151) are included, one for each direction of transmission.

2.03 A J92618S L2 provides one CP 151 to equip the regenerator for additional directional capabilities. One L2 must be provided for each additional direction.

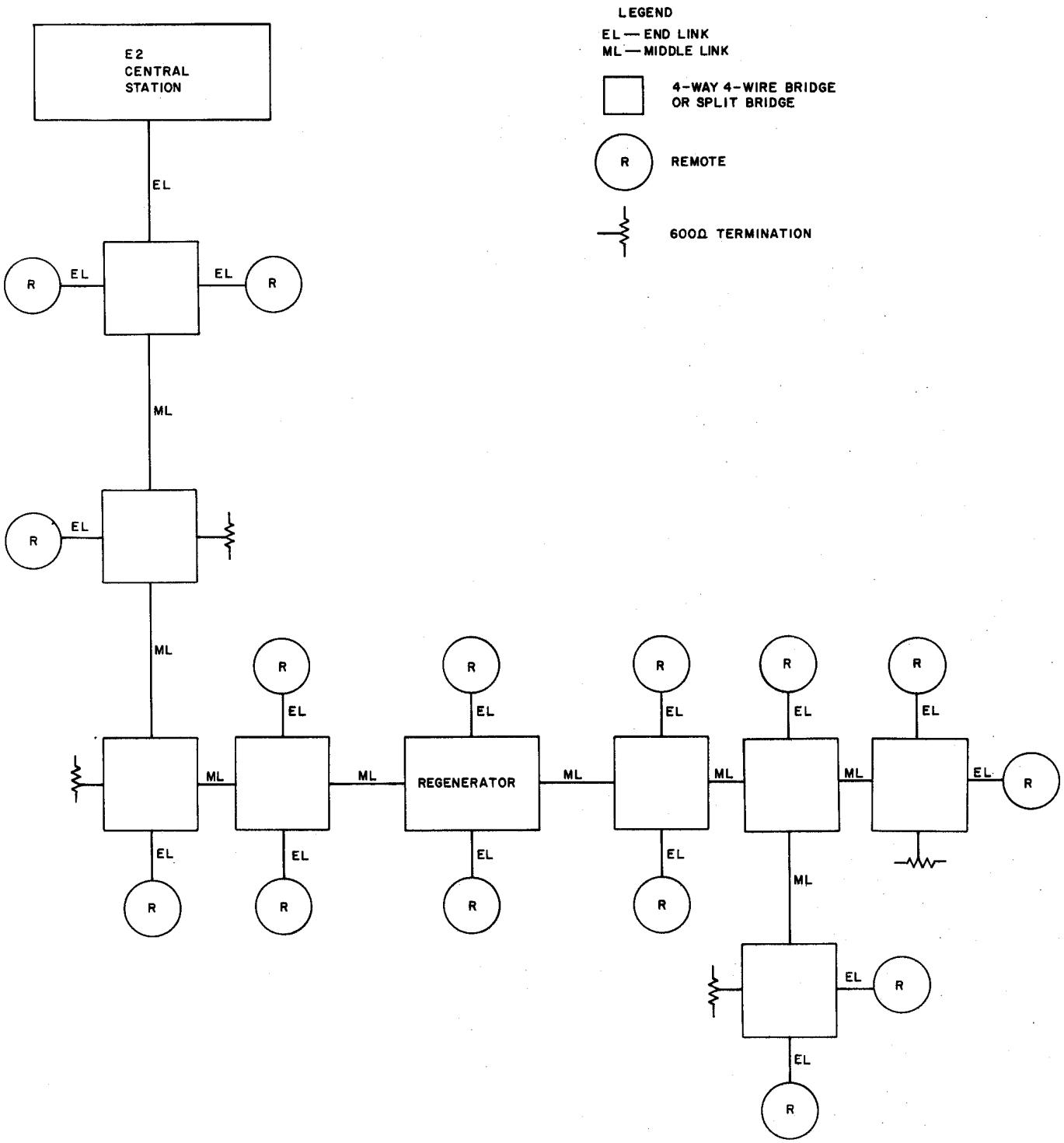


Fig. 1—Typical E2 System Using Regenerator

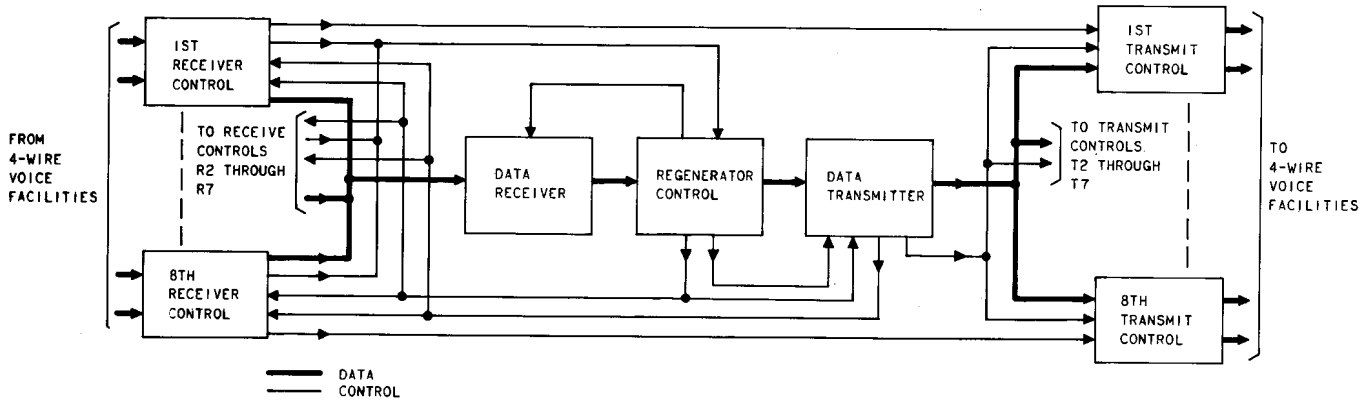


Fig. 2—J92618S Stand-Alone Type Data Regenerator

TABLE A

CP NUMBER	CP NAME	FUNCTION	SD
P/O 151*	Receive Control	Provides tone detection-amplification	1C319-01
P/O 152	Data Receiver	Converts FSK tones to binary voltage levels	1C319-01
153	Logic Control	Retimes and reshapes data	1C319-01
92	Word Length Counter	Provides 31-bit, five-stage counter	1C302-01
90	Shift Register	Provides 6-bit buffer store	1C302-01
88	Clock	Provides timing for regenerator	1C302-01
P/O 152	Data Transmitter	Converts binary voltage levels to FSK tones	1C319-01
P/O 151*	Transmit Control	Provides amplification and gating for reconstructed data	1C319-01

* One CP151 required for each 4-wire facility which terminates in the regenerator.

B. J92618R Collocated Version

2.04 The collocated regenerator-remote version (Fig. 3) consists of five circuit packs, as shown in Table B. The receive control, data receiver, data transmitter, and transmit control circuits are identical to those used in the stand-alone version; the difference is that this circuitry is shared by the regenerator and the E2 remote. This eliminates the need for a data transmission circuit in the remote.

2.05 Additional circuit packs included with the collocated version consists of two cable drivers used to interface the data transmission control (DTC) circuitry of the E2 remote to the regenerator circuitry and a logic interface control which contains a six-stage shift register as well as control circuitry.

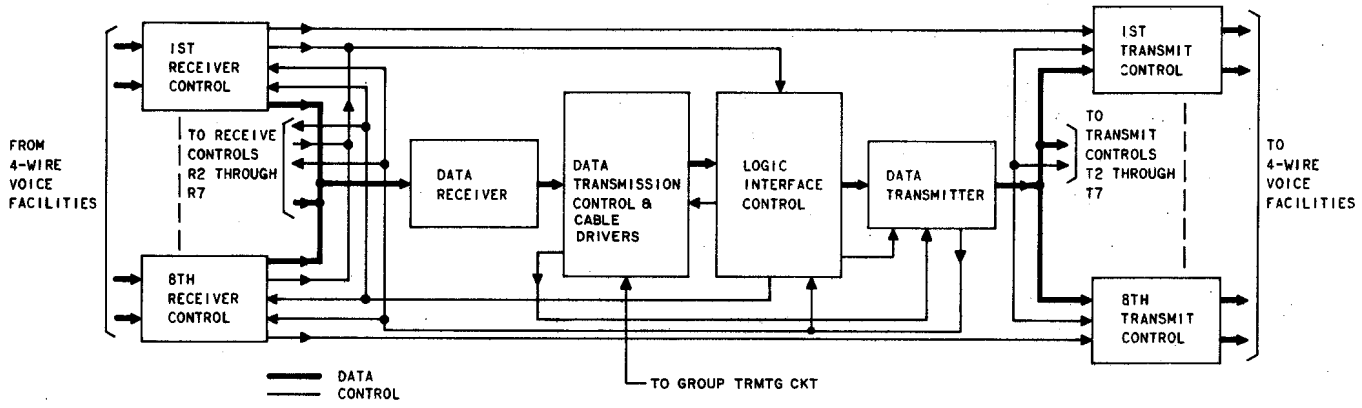


Fig. 3—J92618R Data Regenerator Combined With E2 Remote

TABLE B

CP NUMBER	CP NAME	FUNCTION	SD
P/O 151*	Receive Control	Provides tone detection-amplification	1C319-01
P/O 152	Data Receiver	Converts FSK tones to binary voltage levels	1C319-01
154	Logic Interface Control	Provides 6-bit buffer storage and control of received data	1C319-01
157	Cable Driver	Provides interface between regenerator and data transmission control (DTC)	1C319-01
158	Cable Driver		
P/O 152	Data Transmitter	Converts binary voltage levels to FSK tones	1C319-01
P/O 151*	Transmit Control	Provides amplification and gating for reconstructed data	1C319-01

* One CP 151 required for each 4-wire network terminating in the regenerator.

2.06 The word length counter and clock circuits located in the DTC circuit of the E2 remote are shared by both the remote and the regenerator.

2.07 A J92618R L2 provides one CP 151 to equip the regenerator for additional directional capabilities. One L2 must be provided for each additional direction.

3. FUNCTIONAL DESCRIPTION

3.01 Figure 4 shows a functional block diagram of the regenerator. The incoming data signals, on the RT—RR leads, are first put through a protection-and-filter circuit and then through a limiter circuit. From there, the tone detector senses the data signal and sets the flip-flop in the appropriate receive control circuit which, in turn,

opens the analog gate allowing data to flow to the data receiver circuit. Simultaneously with the opening of the analog gate, the transmit control associated with the receive control is inhibited by signal RM. This stops data from being transmitted back in the direction from which it was received. The data is then passed from the analog gate to the limiter circuit in the data receiver via the R lead. Here the signals are amplified by a second limiter, converting the data tones (1300- and 2100-Hz) from sine waves to square waves. The square waves are then demodulated by the combined action of the differentiator, low-pass filter, and slicer circuitry. As the 1300-Hz and 2100-Hz signals are received by the data receiver, the demodulator circuitry converts these tones into binary voltage levels corresponding to 1s and 0s, respectively. These binary voltage levels are then transmitted to the regenerator control circuit via the RD (received data) lead.

3.02 The regenerator control circuit consists of a clock, a word-length counter, a logic control circuit, and a shift register. After the data receiver's gate has been enabled by the TON pulse, data is allowed to enter the regenerator control circuit. When the zero start bit is detected by the logic control circuit, the shift register is loaded appropriately with a new start sequence. Once loaded, the shift register outputs the start sequence. Note that since the regenerator reconstructs the word start sequence, the system incurs a 6-bit delay (approximately 10 milliseconds) each time a word is passed through the regenerator. Once the start sequence has been transmitted, the regenerated information and parity portions of the word follow. As the word length counter reaches state 31, the logic control is cleared in preparation for the next word. This process continues until all words in the sequence have been regenerated. Note that the regenerator at no time stores a word or any part of a word. The word start sequence is the only part of each word that is totally reconstructed. The remaining information and parity portions of the word are only retimed and reshaped. Errors occurring before regeneration will not be corrected since no error detection or correction circuitry is incorporated into the regenerator.

3.03 As each pulse is shifted out of the shift register, it is transmitted to the data transmitter circuit via the TDR (transmitted data regenerated) lead. Here the binary signals are fed through a level control to the control oscillator. The control oscillator detects the binary output and converts the logic 1s to 1300-Hz tones (marks) and the logic 0s to 2100-Hz tones (spaces). The output from the oscillator is then fed through an emitter-follower circuit to the analog gates in the transmit control circuits via the COS (controlled oscillator) lead. Note that if the data is received on receive control circuit R1, data will not be transmitted from transmit control T1 since it is inhibited by the associated RM lead. All other analog gates are open and data will be transmitted by transmit control circuits T2 through T8. The pulses are then amplified, sent through a protection circuit, and transmitted to the voice facilities via the TR—TT leads.

3.04 The regenerator collocated with an E2 remote operates in a similar manner except that some circuitry in the DTC and regenerator is shared. The 6-bit delay does not hinder the system's operation since the remote is kept from responding until the fully regenerated word has been transmitted.

4. REFERENCES

4.01 The following is a list of the schematic drawings (SDs) and Bell System Practices (BSPs) associated with the multidirectional data regenerator.

DRAWING	TITLE
1C319-01	Multidirectional Data Regenerator
1C302-01	Data Transmission Control Circuit
SECTION	**TITLE**
201-644-100	Overall System—Description
201-644-111	Alarm Reporting Remote—Description
201-644-112	Manual Alarm Central—Description
201-644-113	Status Polling Central—Description
201-644-114	Status Reporting Remote—Decription
314-411-510	E2 Data Network—Maintenance
865-100-101	E2 Data Network—Engineering

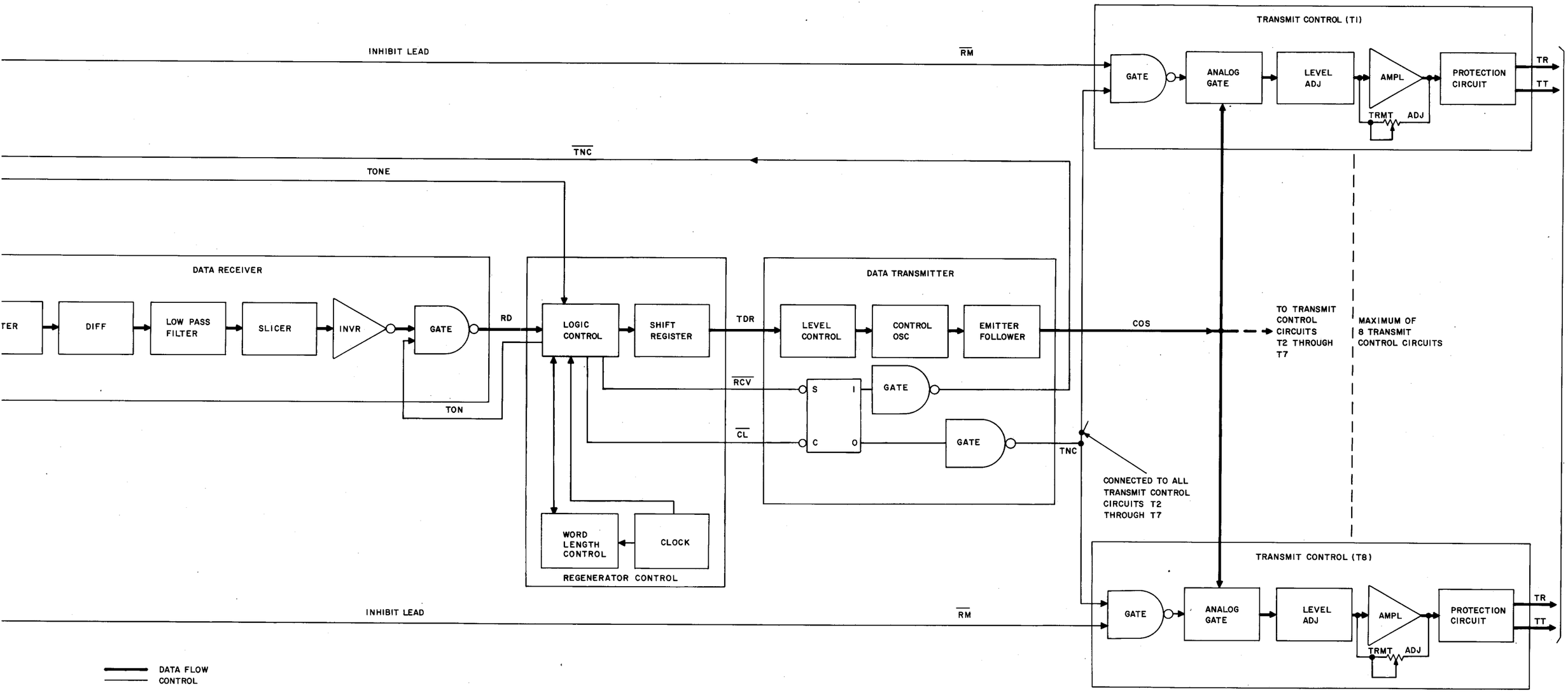
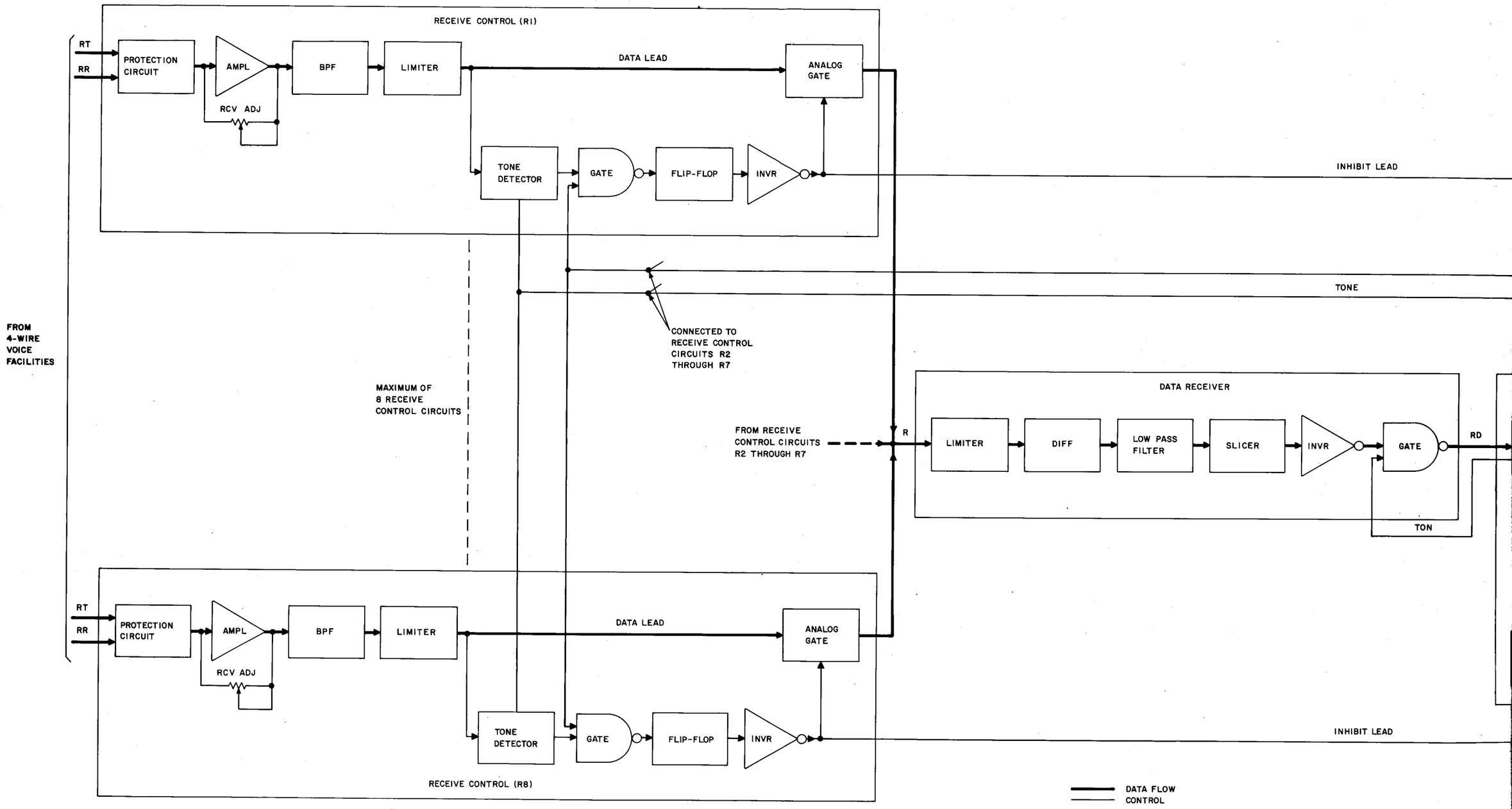


Fig. 4—Data Regenerator Functional Block Diagram


RECEIVE CONTROL (R1)
RT
RR
PROTECTION CIRCUIT
AMPL
RCV ADJ
BPF
LIMITER
DATA LEAD
ANALOG GATE
TONE DETECTOR
GATE
FLIP-FLOP
INVR
INHIBIT LEAD
TONE
FROM 4-WIRE VOICE FACILITIES
CONNECTED TO RECEIVE CONTROL CIRCUITS R2 THROUGH R7
MAXIMUM OF 8 RECEIVE CONTROL CIRCUITS
DATA RECEIVER
FROM RECEIVE CONTROL CIRCUITS R2 THROUGH R7
R
LIMITER
DIFF
LOW PASS FILTER
SLICER
INVR
GATE
RD
TON
RT
RR
PROTECTION CIRCUIT
AMPL
RCV ADJ
BPF
LIMITER
DATA LEAD
ANALOG GATE
TONE DETECTOR
GATE
FLIP-FLOP
INVR
INHIBIT LEAD
RECEIVE CONTROL (R8)
DATA FLOW
CONTROL